What is claimed is:

1. A method of providing thermal stress relieve for packages that are used for the mounting of semiconductor devices, comprising the steps of:

providing a circuit board on the surface of which at least one point of electrical contact has been provided;

forming one or more layers of thermal stress relieve material on the surface of said circuit board;

providing one or more semiconductor devices for mounting on said circuit board said semiconductor devices having been provided with points of electrical contact; and

establishing electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices.

2. The method of claim 1 wherein said semiconductor devices are flip chip devices whereby said flip chip devices have been provided with solder bumps for electrical interconnect of said flip chips with surrounding electrical circuitry or components.

3. The method of claim 1 wherein said circuit board is a Printed Circuit Board.

4. The method of claim 1 wherein said thermal stress relieve material comprises Elastomer or any other Thermal Compliant material.

5. The method of claim 1 wherein said establishing electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices comprises methods of Printed Circuit Board technology for establishing electrical contact between overlying points of electrical contact or methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact.

6. The method of claim 5 wherein said methods of Printed Circuit Board technology for establishing electrical contact between overlying points of electrical contact comprise:

creating one or more openings in said created layers of thermal stress relieve material whereby said openings align with one or more overlying points of electrical contact on the surface of one or more created layers of said thermal stress relieve material;

depositing a layer of conductive material over said created layers of thermal stress relieve material, including said openings; and

patterning and etching said layer of conductive material, forming a upper layer of interconnect lines and contact pads on the surface of said created layer of said thermal stress relieve material, partially exposing the surface of said thermal stress relieve material.

7. The method of claim 6 wherein said creating one or more openings in said created layers of thermal stress relieve material comprises methods of photolithography.

8. The method of claim 6 wherein said depositing a layer of conductive material over said created layers of thermal stress relieve material comprises steps of electroless seeding followed by electroplating of the surface of said created layers of said thermal stress relieve material.

9. The method of claim 6 with the additional steps of:

depositing a layer of dielectric over said upper layer of interconnect lines, including the surface of said partially exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric to open an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

10. The method of claim 9 with the additional steps of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

11. The method of claim 5 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads being created on an

underlying layer of thermal stress relieve material, comprising the steps of:

depositing a first layer of conductive material on the surface of said underlying layer of created layer of thermal stress relieve material;

pattering and etching said first layer of conductive material, creating a first pattern of interconnect lines or contact pads;

creating a layer of thermal stress relieve material on the surface of said underlying layer of thermal stress relieve material including said first pattern of interconnect lines or contact pads;

creating vias in said layer of stress relieve material, said vias overlying interconnect lines or contact pads to which said electrical contact is to be established;

depositing a second layer of conductive material on the surface of said layer of stress relieve material, including said vias, connecting said second layer of conductive material to said first pattern of interconnect lines or contact pads; and

pattering and etching said second layer of conductive material, creating a second pattern of interconnect lines or contact pads partially exposing the surface of said created layer of thermal stress relieve material.

12. The method of claim 11 wherein said creation of vias comprises methods of lithographic etching or laser drilling.

13. The method of claim 11 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is applied one or more times during said step of creating a layer of thermal stress relieve material on the surface of said circuit board, creating multiple overlying vias that interconnect multiple layers of interconnect lines and contact pads.

14. The method of claim 11 wherein said depositing a first layer of conductive material comprises steps of electroless seeding followed by electroplating of the surface of said underlying layer of said thermal stress relieve material.

15. The method of claim 11 wherein said depositing a second layer of conductive material comprises steps of electroless seeding followed by electroplating of the surface of said created layer of said thermal stress relieve material said step of electroless seeding followed by electroplating to be performed after said creation of vias in said created layer of thermal stress relieve material.

16. The method of claim 11 with the additional steps of:

depositing a layer of dielectric over said second layer of conductive material, including the surface of said partially exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric to open an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

17. The method of claim 16 with the additional steps of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

18. The method of claim 1 with the additional step of treating one or more of said created layers of thermal stress relieve material by methods of etching or swelling to roughen the surface of said created layers and thereby promote adhesion for a subsequent electroless metal deposition said additional step to be performed after said step of creating a layer of thermal stress relieve material.

19. The method of claim 1 with the additional step of curing one or more of said created layers of thermal stress relieve material said additional step to be performed after said step of creating a layer of thermal stress relieve material.

20. The method of claim 19 wherein said curing is thermal curing.

21. The method of claim 19 wherein said curing is E-beam curing.

22. The method of claim 19 wherein said curing is UV curing.

23. The method of claim 1 wherein establishing electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices is providing contact pads on the surface of said created layers of thermal stress relieve material, said contact pads having been connected to at least one

of said points of electrical contact provided on the surface of said circuit board, said contact pads further being points of electrical contact for said semiconductor devices.

24. The method of claim 1 wherein establishing electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices is providing at least one conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact provided on the surface of said circuit board using interconnect methods of PCB technology or Build Up Board technology, said conducting interconnects further being points of electrical contact for said semiconductor devices.

25. The method of claim 1 wherein establishing electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices is providing at least one contact pad on the surface of said created layers of thermal stress relieve material in addition to providing at least one conducting interconnect through said created layers of thermal stress relieve material, said contact pads on the surface of said

created layers of thermal stress relieve material having been connected to at least one of said conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact points provided on the surface of said circuit board using interconnect methods of PCB technology or Build Up Board technology, said contact pads on the surface of said created layers of thermal stress relieve material being points of electrical contact for said semiconductor devices.

26. The method of claim 25 wherein providing at least one contact pad on the surface of said created layers of thermal stress relieve material comprises the steps of:

depositing a layer of conducting material over the surface of said created layer of thermal stress relieve material;

patterning and etching said layer of conducting material, creating a pattern of interconnect lines on the surface of said created layer of thermal stress relieve material, partially exposing said thermal stress relieve material;

depositing a layer of dielectric over the surface of said pattern of interconnect lines, including the surface of said partially exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric to open an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

27. The method of claim 26 with the additional steps of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

28. The method of claim 5 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of

interconnect lines and contact pads being created on a BGA surface, comprising the steps of:

providing a semiconductor surface having been provided with points of electrical contact in its surface;

creating a layer of thermal stress relieve material on the surface of said semiconductor surface;

creating vias in said layer of stress relieve material, said vias overlying said points of electrical contact provided in the surface of said semiconductor surface;

depositing a layer of conductive material on the surface of said layer of stress relieve material, including said vias, connecting said layer of conductive material to electrical contact provided in said semiconductor surface; and

pattering and etching said layer of conductive material, creating a pattern of interconnect lines or contact pads, partially exposing the surface of said created layer of thermal stress relieve material.

29. The method of claim 28 wherein said semiconductor surface is the surface of a BGA substrate.

30. The method of claim 28 wherein said creation of vias comprises methods of lithographic etching or laser drilling.

31. The method of claim 28 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is applied one time during said step of creating a layer of thermal stress relieve material on the surface of said semiconductor surface, creating a first created layer of thermal stress relieve material on said semiconductor surface.

32. The method of claim 28 wherein said depositing a layer of conductive material comprises steps of electroless seeding followed by electroplating of the surface of said underlying layer of said thermal stress relieve material said steps of electroless seeding followed by electroplating to be performed after said creation of vias in said created layer of thermal stress relieve material.

33. The method of claim 28 with the additional steps of:

depositing a layer of dielectric over said pattered layer of conductive material, including the surface of said partially exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric to open an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board,

said conductive pads further being points of electrical contact for said semiconductor devices.

34. The method of claim 33 with the additional steps of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

35. A structure for providing thermal stress relieve for packages that are used for the mounting of semiconductor devices, comprising:

a circuit board on the surface of which at least one point of electrical contact has been provided;

one or more layers of thermal stress relieve material created on the surface of said circuit board;

one or more semiconductor devices for mounting on said circuit board said semiconductor devices having been provided with points of electrical contact; and

electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices.

36. The structure of claim 35 wherein said semiconductor devices are flip chip devices whereby said flip chip devices have been provided with solder bumps for electrical interconnect of said flip chips with surrounding electrical circuitry or components.

37. The structure of claim 35 wherein said circuit board is a Printed Circuit Board.

38. The structure of claim 35 wherein said thermal stress relieve material comprises Elastomer or any other Thermal Compliant material.

39. The structure of claim 35 wherein said electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices is established using methods of Printed Circuit Board technology for establishing electrical contact between overlying points of electrical contact or methods of Build Up Board technology for establishing

electrical contact between overlying points of electrical contact.

40. The structure of claim 39 wherein said methods of Printed Circuit Board technology for establishing electrical contact between overlying points of electrical contact comprise:

creating one or more openings in said created layers of thermal stress relieve material whereby said openings align with one or more overlying points of electrical contact on the surface of one or more created layers of said thermal stress relieve material;

depositing a layer of conductive material over said created layers of thermal stress relieve material, including said openings; and

creating an upper layer of interconnect lines and contact pads formed by methods of patterning and etching said layer of conductive material on the surface of said created layer of said thermal stress relieve material, partially exposing the surface of said thermal stress relieve material.

41. The structure of claim 40 wherein said one or more openings in said created layers of thermal stress relieve material are created using methods of photolithography.

42. The structure of claim 40 wherein said layer of conductive material over said created layers of thermal stress relieve material is deposited using steps of electroless seeding followed by electroplating of the surface of said created layers of said thermal stress relieve material.

43. The structure of claim 40 with the addition of:

a layer of dielectric deposited over said upper layer of interconnect lines, including the surface of said partially exposed thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

44. The structure of claim 43 with the addition of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

45. The structure of claim 39 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads being created on an underlying layer of thermal stress relieve material, comprising the steps of:

depositing a first layer of conductive material on the surface of said underlying layer of created layer of thermal stress relieve material;

pattering and etching said first layer of conductive material, creating a first pattern of interconnect lines or contact pads;

creating a layer of thermal stress relieve material on the surface of said underlying layer of thermal stress relieve material including said first pattern of interconnect lines or contact pads;

creating vias in said layer of stress relieve material, said vias overlying interconnect lines or contact pads to which said electrical contact is to be established;

depositing a second layer of conductive material on the surface of said layer of stress relieve material, including said vias, connecting said second layer of conductive material to said first pattern of interconnect lines or contact pads; and

pattering and etching said second layer of conductive material, creating a second pattern of interconnect lines or contact pads partially exposing the surface of said created layer of thermal stress relieve material.

46. The structure of claim 45 wherein said creation of vias comprises methods of lithographic etching or laser drilling.

47. The structure of claim 45 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is applied one or more times during said step of creating a layer of thermal stress relieve material on the surface of said circuit board, creating multiple overlying vias that interconnect multiple layers of interconnect lines and contact pads.

48. The structure of claim 45 wherein said depositing a first layer of conductive material comprises steps of electroless seeding followed by electroplating of the surface of said underlying layer of said thermal stress relieve material.

49. The structure of claim 45 wherein said depositing a second layer of conductive material comprises steps of electroless seeding followed by electroplating of the surface of said created layer of said thermal stress relieve material said step of electroless seeding followed by electroplating to be performed after said creation of vias in said created layer of thermal stress relieve material.

50. The structure of claim 45 with the addition of:

a layer of dielectric deposited over said second layer of conductive material, including the surface of said partially exposed thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

51. The structure of claim 50 with the addition of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

52. The structure of claim 35 with the addition of treating one or more of said created layers of thermal stress relieve material by methods of etching or swelling to roughen the surface of said created layers and thereby promote adhesion for a subsequent electroless metal deposition said additional step to be performed after said step of creating a layer of thermal stress relieve material.

53. The structure of claim 35 with the addition of curing one or more of said created layers of thermal stress relieve material said additional step to be performed after said step of creating a layer of thermal stress relieve material.

54. The structure of claim 53 wherein said curing is thermal curing.

55. The structure of claim 53 wherein said curing is E-beam curing.

56. The structure of claim 53 wherein said curing is UV curing.

57. The structure of claim 35 wherein electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices is established by providing contact pads on the surface of said created layers of thermal stress relieve material, said contact pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said contact pads further being points of electrical contact for said semiconductor devices.

58. The structure of claim 35 wherein electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices is established by providing at least one conducting interconnect through said created layers of

thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact provided on the surface of said circuit board using interconnect methods of PCB technology or Build Up Board technology, said conducting interconnects further being points of electrical contact for said semiconductor devices.

59. The structure of claim 35 wherein electrical contact between said point of electrical contact provided in the surface of said circuit board and said points of electrical contact provided in said semiconductor devices is established by providing at least one contact pad on the surface of said created layers of thermal stress relieve material in addition to providing at least one conducting interconnect through said created layers of thermal stress relieve material, said contact pads on the surface of said created layers of thermal stress relieve material having been connected to at least one of said conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact points provided on the surface of said circuit board using interconnect methods of PCB technology or Build Up Board technology, said contact pads on the surface of said created layers of thermal stress relieve material

being points of electrical contact for said semiconductor devices.

60. The structure of claim 59 wherein at least one contact pad on the surface of said created layers of thermal stress relieve material is provided comprising the steps of:

depositing a layer of conducting material over the surface of said created layer of thermal stress relieve material;

patterning and etching said layer of conducting material, creating a pattern of interconnect lines on the surface of said created layer of thermal stress relieve material, partially exposing said thermal stress relieve material;

depositing a layer of dielectric over the surface of said pattern of interconnect lines, including the surface of said partially exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric to open an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

61. The structure of claim 60 with the addition of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

62. The structure of claim 39 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads being created on a BGA surface, comprising the steps of:

providing a semiconductor surface having been provided with points of electrical contact in its surface;

creating a layer of thermal stress relieve material on the surface of said semiconductor surface;

creating vias in said layer of stress relieve material, said vias overlying said points of electrical contact provided in the surface of said semiconductor surface;

depositing a layer of conductive material on the surface of said layer of stress relieve material, including said vias, connecting said layer of conductive material to electrical contact provided in said semiconductor surface; and

pattering and etching said layer of conductive material, creating a pattern of interconnect lines or contact pads, partially exposing the surface of said created layer of thermal stress relieve material.

63. The structure of claim 62 wherein said semiconductor surface is the surface of a BGA substrate.

64. The structure of claim 62 wherein said vias are created comprising methods of lithographic etching or laser drilling.

65. The structure of claim 62 wherein said methods of Build Up Board technology for establishing electrical contact between overlying points of electrical contact is applied one time during said step of creating a layer of thermal stress relieve material on the surface of said semiconductor surface, creating a first created layer of thermal stress relieve material on said semiconductor surface.

66. The structure of claim 62 wherein said depositing a layer of conductive material comprises steps of electroless seeding followed by electroplating of the surface of said underlying layer of said thermal stress relieve material said steps of electroless seeding followed by electroplating to be performed after said creation of vias in said created layer of thermal stress relieve material.

67. The structure of claim 66 with the addition of:

a layer of dielectric deposited over said pattered layer of conductive material, including the surface of said partially exposed thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on the surface of said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

68. The structure of claim 67 with the addition of:

positioning said semiconductor devices above said circuit board such that said array of conductive pads in the layer of

dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by methods of thermal reflow or any other method to connect points of electrical contact for said semiconductor devices with said array of conductive pads.

69. The method of claim 1 wherein said creating one or more layers of thermal stress relieve material on the surface of said circuit board is a laminating process.

70. The method of claim 1 wherein said creating one or more layers of thermal stress relieve material on the surface of said circuit board is a liquid depositing process.

71. The structure of claim 35 wherein said one or more layers of thermal stress relieve material created on the surface of said circuit board uses a laminating process.

72. The structure of claim 35 wherein said one or more layers of thermal stress relieve material created on the surface of said circuit board uses a liquid depositing process.